DETAILED ACTION

1. Claims 1,3-13, 15-24 remain pending in the current application and have been examined.

Response to Arguments

2. Applicant's arguments filed 01/17/2008, with respect to 1, 10, 13 and 22 have been fully considered and are persuasive. The Non-Final Rejection of 08/17/2007 has been withdrawn.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Scott A. Ouellette on 04/11/2008.

The application has been amended as follows:

Claim 1, line 17, change "may transmit" to "transmits".

Claim 1, line 18, change the last period "." to a semicolon ";".

Claim 1, after line 18, add the following:

wherein the first logic section comprises built-in-self-test (BIST) logic and the one or more test-related signals comprise test input signals for use in testing the SUT.

Cancel **Claim 2**.

Claim 7, line 3, change “may receive” to “receives”.

Claim 7, line 5, change “may compare” to compares”.

Claim 10, line 3, change the semicolon “;” to “comprising programmable built-in-self-test logic;”.

Claim 10, line 17, change “may transmit” to “transmits”.

Claim 12, line 2, delete “the first logic section comprises programmable built-in-self-test logic and”.

Claim 13, line 18, change the last period “.” to a semicolon ";".

Claim 13, after line 18, add the following:

wherein the first logic section comprises built-in-self-test (BIST) logic and the one or more test-related signals comprise test input signals for use in testing the SUT.

Cancel **Claim 14**.

Claim 22, line 1, change “system that may be used to” to “system to”.

Claim 22, line 2, change "a first logic section” to “a first logic section comprising programmable built-in-self-test logic”.

Claim 24, line 2, delete “the first logic section comprises programmable built-in-self-test logic and”.

Allowable Subject Matter

4. Claims 1,3-13, 15-24 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to a system to test the functionality/operation of at least one system-under-test.

The claimed invention as set forth in **claim 1** (broadest claim) recites features such as:

Testing system for use in testing a system-under-test (SUT), the testing system comprising:

a first logic section that transmits one or more test-related signals for use during a test mode of the SUT;

a second logic section that transmits one or more other signals during a normal operating mode of the SUT; and

a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

wherein:

when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section transmits the one or more other signals to the SUT,

wherein the first logic section comprises built-in-self-test (BIST) logic and the one or more test-related signals comprise test input signals for use in testing the SUT.

The prior arts of record teach a *single control signal,* the "test mode" signal input to the initial logic 46, which determines which of the "'other components" and the BIST 40 are coupled to the RAM 42. When the test mode signal is "low", the "other components" are coupled to the RAM 42 through multiplexer 44 and when the test mode signal is "high", the BIST 40 is coupled to the RAM 42 through multiplexer 44; **Jamal** (US-5572712) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination:

a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

wherein:

when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section transmits the one or more other signals to the SUT;

As such, modification of the prior art of record to include the claimed *third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals and the claimed connectivity thereof* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals and the claimed connectivity thereof* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective states of two control signals and the claimed connectivity thereof* as set forth in **claim 1**. Independent **clams 10, 13 and 22** recite similar patentable features and are allow for the same reasons as **claim 1**. Hence, **claims 1, 3-13, 15-24** are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of **claims 1,**

3-13, 15-24. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. TABONE JR whose telephone number is (571)272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117

/John J. Tabone, Jr./
Examiner
Art Unit 2117 4/11/2008